

Aerospace and defense

## Leonardo Leverages Xpedition, HyperLynx and Valor for Right-the-First-Time Mil-Aero Innovations

### Product

Xpedition, HyperLynx, Valor

### Business challenges

Perform the complex routing required for many high-speed nets to FPGAs

Ensure design development matches completely with signal integrity analysis

Simultaneously analyze the power integrity of the layers and decoupling capacitors, and verify boards through thermal analysis

### Keys to success

Concurrent engineering and layout

Cross-probing between design and constraints

Design validation and verification and DFM validation

Advanced processes such as reuse

### Results

From 2 to 3 respins to right the first time innovation

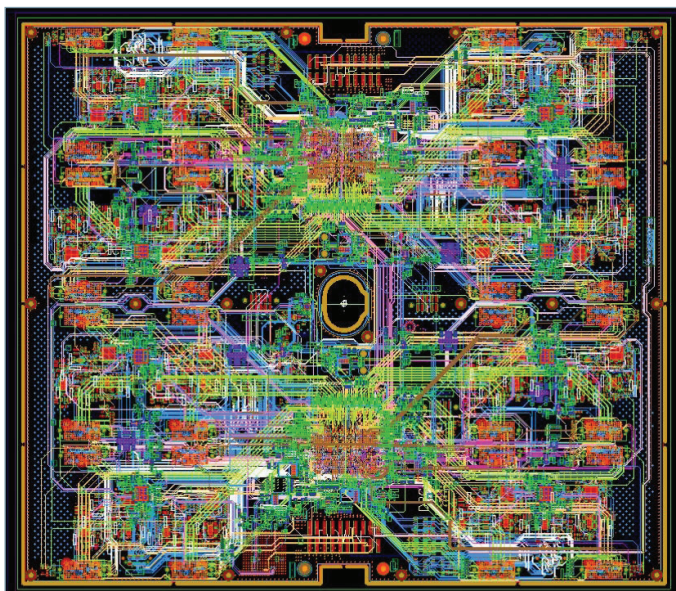
Hierarchical development made possible the widest and most highly populated boards the company has ever created

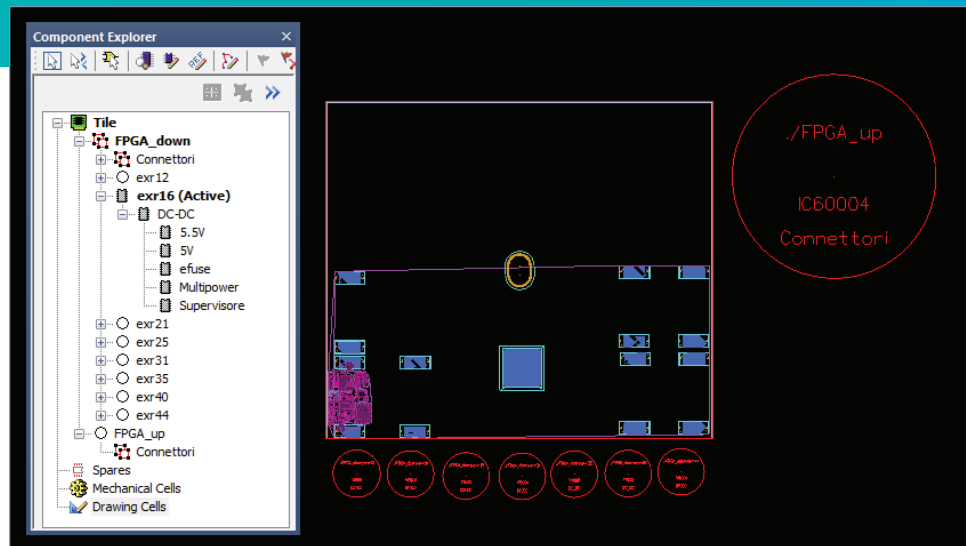
Leonardo (electronics division – Rome Italy) operates in a unique market segment, as it serves a wide range of customers, from private-sector companies, to governments and public institutions, and armed forces and intelligence agencies. For these very different types of customers, Leonardo designs and creates a wide range of products, systems, services and integrated solutions tailored to their customers' needs in defence, protection, and security. An ongoing challenge for the company is that it must produce systems that operate in different environments, such as air and land, naval and maritime, space and cyberspace, and of course each product comes with its own special requirements. To

address these design challenges and get right-the-first-time innovations to customers quickly, the company uses the Xpedition®, HyperLynx® and Valor® tool portfolios from Siemens EDA.

### Coping with the Market Challenges

Leonardo emphasizes meeting time-to-market requirements, and being a Tier-1 company, that is required to develop high-quality, long lasting products. For that, the company invests a significant part of its revenue in cutting-edge technologies to support it in developing its radars, radios, electro-optical systems, combat management systems, and especially their AESA (Active Electronic Scanning Antenna) radar.





Internally, the company promotes the “Leonardo innovation award” to drive teams to develop their skills and competencies. These strategies help Leonardo in facing its competition in this segment.

“Systems are becoming increasingly complex and integrated, as the same board contains more and more functions,” says a team member at Leonardo. “The engineers must have multiple skills to cover the project needs and have to be able to set up the tools to keep constraints under control. Tools became essential for our engineers, to aid them in their new challenges. In our business the trend is moving the processing closer to the antenna and, at the end, to put it into the antenna. It means we will develop boards that have even more integrated systems, with even more complex functions, that must work in very hard environment. So mechanical, thermal and SI/PI studies drive our solutions.”

#### Leonardo’s Design and Product Development Challenges

Leonardo’s products are mainly multi-board projects that include analog and digital programmable devices, with high-speed communication lanes and high-efficiency DC/DC converters close to analog nets.

Because of the programmable digital devices and the high pin density of its packages, Leonardo’s boards have many layers, between 14 and 22. The size of its boards is also variable, depending on the system, with a range of 7200mm<sup>2</sup> to 106000mm<sup>2</sup>. The typical high-speed lane maximum transfer data is 5Gbs. Their complex boards can have 133 differential nets and up to 4000 components with 18000 connections. The protocols on Leonardo’s boards are usually proprietary, but when the company does use standard protocols, it uses SRIO, JESD204, or PCIe.

*“With hierarchical design and IP reuse, we reduced to 1/3 the schematic drawing time, and to 1/2 the layout drawing time. We also reduced the risk of mistakes and the checking time.”*

In designing these complex boards, Leonardo faces a spectrum of challenges ranging from ensuring signal and power integrity, to manufacturability, meeting reliability and cost requirements, and up to providing higher functions with increased thermal density successfully. With its high-speed, high-power designs, it must find the right trade-offs between power distribution, electrical, and performance. Its electro-mechanical designs require 3D mechanical checks between the daughter boards and the main boards, and to meet its project time constraints, it creates a hierarchical schematic, which allows it to reduce a third of the time required for the schematic and half the time required for layout design.

The designer's biggest challenge remains in the complex routing required for their many high-speed nets to the FPGA. For that, it must make sure its design development matches completely with signal integrity analysis. Also, to support the high number of transceivers used in its designs, it must simultaneously analyse the power integrity of the layers and decoupling capacitors, and its boards must be verified through thermal analysis, as well.

To address these challenges, Leonardo is taking full advantage of the technologies available to it from the Siemens Xpedition portfolio. One of the most useful capabilities is Xpedition's ability to use hierarchical development, which made it possible for its designer to design the widest and most highly populated board that the company has ever created. The company also found the reuse of IP to be another key capability that helped it meet its challenges.

Then, after routing the most meaningful net of the project, Leonardo performed signal integrity analysis to validate it and make sure all the requirements are met. To keep the electrical characteristics of the

high-speed nets under control while routing all the others, Leonardo engineers generated rules for HyperLynx DRC and tailored it to their project.

In the near future, they expect to implement thermal analysis and FPGA I/O optimization at the engineering level as well.

### **Best-Practices Q&A with Leonardo**

*How do you collaborate across your multi-discipline team?*

During electrical engineering/layout, we use concurrent development, and we also run electro/mechanical/thermal verifications at different design stages.

*Have you been able to meet your target design time goals? How?*

Even if our schedule is very short and the project huge, we meet our goals by planning our iteration between drawing the layout and simulating the net from the beginning. After getting validation from the simulation team, we freeze the simulated nets and go on with the other nets, controlling any change using the DRC.

*How do you minimize design iterations and ensure quality products?*

#### **Schematic Design:**

We begin by putting as much information as possible into the Constraint Manager. In this preliminary step, it is fundamental to decide for each net class which are the planes assigned and the dimensions of the net to keep the impedance as near as possible to the ideal. This is also the best time to review the stackup. It is also useful to perform some preliminary simulations with HyperLynx to validate the stackup. Next, we organize a priority order for the routing and tailor the rules for HyperLynx DRC. In particular, we assign the rules to the class net. Then we route the nets following the established priority. Then we

## Solutions/Services

Xpedition Enterprise  
HyperLynx SI/PI/DRC  
Valor NPI  
[siemens.com/eda](https://www.siemens.com/eda)

## Customer's primary business

One of the world's major players in aerospace, defense and security, Leonardo delivers cutting-edge and dual-use technologies, meeting both military and civil requirements for governments, institutions, and business customers.  
[www.leonardocompany.com](https://www.leonardocompany.com)

## Customer location

Rome  
Italy

perform additional simulation using HyperLynx on the routed net to confirm the preliminary simulation and, after this, freeze the nets and keep them under the control of HyperLynx DRC while routing the others. This practice seems to be a good fit for our requirements and to minimize the design iterations.

### Layout Design:

Multiple DRC checks during the PCB layout phase, including 2D, 3D and electrical checks, are necessary. Then we define specific constraints for the FPGA and daughter board. We make extended use of the grouping through hierarchical cluster definitions, which allows us to duplicate a verified part of the circuit to reduce design time. We then perform copper balancing, with special attention to covering manufacturing requirements, and verify trace impedance with HyperLynx DRC. Finally, we use the design for fabrication (DFF) manufacturability check with Valor NPI.

### When/how often were analyses run during the design process?

Some analyses are performed at the beginning to define the best stackup, as an error at this point could compromise everything. During the routing of the PCB, we performed some simulations at the beginning to validate the preliminary ones, but more important are the simulations performed in the middle and at the end of routing. The DRC analysis should be performed on net class by net class during routing.

### How would you describe the value of the Xpedition flow (including HyperLynx)?

New technologies need sophisticated tools to manage all the needed constraints. Things that could have been done in the past using experience and skills now also need the support of specific tools like HyperLynx and Xpedition.

### How would you describe the success of recent designs with the Xpedition flow?

People involved in this project accepted the challenges of using new tools to achieve the project requirements. This achievement also had a lot to do with the local Siemens support, especially for the release transition and for the HyperLynx implementation.

We pushed the Xpedition flow to the limits, and this project's requirements forced us to explore, test and use the new release's capabilities that are now part of our "know how". Based on our experience, the other teams are now also using Xpedition and HyperLynx.

### Have you seen a reduction in the number of prototypes using this flow?

A project with this complexity, in the past, could require at least 2–3 respins before having a full functionality release. In this case, we were able to get it **right the first time**.



For more information on **Xpedition, HyperLynx, or Valor**, please contact us at: **949.481.3267 | [info@saratech.com](mailto:info@saratech.com) | [saratech.com](https://www.saratech.com)**

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